EXHIBIT A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

151. (Amended) A synchronous memory device including an array of memory cells, the synchronous memory device comprises:

clock receiver circuitry to receive an external clock signal;

input receiver circuitry to sample a first operation code [synchronously with respect] in response to a rising edge transition of the external clock signal;

a programmable register to store a value which is representative of an amount of time to transpire before the memory device outputs data, wherein the memory device stores the value in the programmable register in response to the first operation code; and

output driver circuitry to output data in response to a second operation code, wherein the data is output after the amount of time transpires, and wherein:

the output driver circuitry outputs a first portion of the data synchronously with respect to a rising edge transition of the external clock signal and outputs a second portion of the data synchronously with respect to a falling edge transition of the external clock signal.

154. (Amended) The memory device of claim 151 wherein the memory device is a synchronous dynamic random access memory [DRAM].

155. (Amended) The memory device of claim 151 wherein the input receiver circuitry receives the second operation code and address information [corresponding to at least one memory cell location of the array of memory cells].

156. (Amended) The memory device of claim 155 [151] wherein the input receiver circuitry receives [at least one of] the second operation code and the address information on consecutive clock cycles of the external clock signal [corresponding to at least one memory cell location of the array of memory cells].

157. (Amended) The memory device of claim 151 wherein the amount of time is [representative of] a number of clock cycles of the external clock signal.

159. (Amended) The memory device of claim 158 wherein the input receiver circuitry receives the third operation code and address information [corresponding to at least one memory cell location of the array of memory cells].

160. (Amended) The memory device of claim 151 further including delay lock loop circuitry coupled to the clock receiver circuitry to generate a first internal clock signal, wherein the data is output in response to [using] the first internal clock signal.

162. (Amended) The memory device of claim 161 wherein the bus includes a set of signal lines [used] to carry [transmit] multiplexed address information, data and control information.

163. (Amended) A method of operation of a synchronous memory device, wherein the memory device includes an array of memory cells and a programmable register, the method of operation of the memory device comprises:

sampling a first operation code synchronously with respect to an external clock signal;

receiving a binary value which is representative of an amount of time to transpire before the memory device outputs data in response to a second operation code wherein the memory device stores the binary value in the programmable register in response to the first operation code [wherein the binary value is representative of an amount of time to transpire before the memory device outputs data in response to a second operation code];

sampling the second operation code; and

outputting the data after the amount of time transpires, wherein a first portion of the data is output synchronously with respect to a first transition of the external clock signal and a second portion of the data is output synchronously with respect to a second transition of the external clock signal.

174. (Amended) The method of claim 163 wherein the memory device [samples the first operation code from an external bus, and wherein the memory device] outputs the data onto an [the] external bus.

175. (Amended) The method of claim 174 wherein the external bus includes a set of signal lines [used] to carry [transmit] multiplexed address information, data and control information.

176. (Amended) A method of controlling a synchronous memory device by a memory controller, wherein the memory device includes an array of memory cells and a programmable register, the method of controlling the memory device comprises:

providing [issuing] a first operation code to the memory device, wherein the first operation code initiates an access of the programmable register in the memory device in order to store a binary value;

providing the binary value to the memory device, wherein the memory device stores the binary value in the programmable register in response to the first operation code;

providing [issuing] a second operation code to the memory device, wherein the second operation code instructs the memory device to accept data that is issued by the memory controller;

providing [issuing] a first portion of the data to the memory device [synchronously with respect to a first] in response to a rising edge transition of the external clock signal; and

providing [issuing] a second portion of the data to the memory

device [synchronously with respect to a second] in response to a falling edge transition of the external clock signal.

177. (Amended) The method of claim 176 wherein the binary value is representative of a delay time to transpire before the memory device samples the data, and wherein the first portion of the data is [issued] provided to the memory device after the delay time transpires.

178. (Amended) The method of claim 176 wherein the binary value is representative of a number of clock cycles of the external clock signal to transpire before the memory device samples the data, and wherein the first portion of the data is provided to the memory device after the delay time transpires.

179. (Amended) The method of claim 176 wherein the binary value is representative of a delay time to transpire before the memory device outputs data in response to an operation code which instructs the memory device to output data[the first transition of the external clock signal is a rising edge transition and the second transition of the external clock signal is a falling edge transition].

183. (Amended) The method of claim 176 wherein the first operation code and the data are [issued onto] provided to the memory device via an external bus.

184. (Amended) The method of claim 183 wherein the external bus includes a set of signal lines used to carry [transmit] multiplexed address information, the data and control information.

186. (Amended) A synchronous memory device, wherein the memory device includes an array of memory cells, the memory device comprises:

input receiver circuitry to sample a first operation code [synchronously with respect] in response to a first transition of an external clock signal;

a programmable register to store a binary value in response to the first operation code, wherein the binary value is representative of an amount of time to transpire before the memory device outputs data; and

output driver circuitry to output data in response to a second operation code and after the amount of time transpires, wherein a first portion of the data is output [synchronously with respect]in response to a second [first] transition of the external clock signal and a second portion of the data is output [synchronously with respect] in response to a third [second] transition of the external clock signal.

[188. The memory device of claim 187 wherein the binary value is representative of a fractional number of clock cycles of the external clock signal.]

188. (Amended) The memory device of claim 186 wherein the [first] second transition of the external clock signal is a rising edge transition and the [second] third transition of the external clock signal is a falling edge transition.

189. (Amended) The memory device of claim 188 wherein the [first and] second and third transitions of the external clock signal are consecutive transitions.

192. (Amended) The memory device of claim 186 further including delay lock loop circuitry to generate a first internal clock signal, wherein the data is output [using] in response to the first internal clock signal.

193. (Amended) The memory device of claim 186 wherein the input receiver circuitry receives address information [corresponding to at least one memory cell location of the array of memory cells].

194. (Amended) The memory device of claim 186 wherein the output driver circuitry outputs the data onto an external bus having a set of signal lines used to [transmit] carry multiplexed address information, the data and control information.

197. (Amended) The memory device of claim 186 wherein the memory device is a synchronous dynamic random access memory [DRAM].